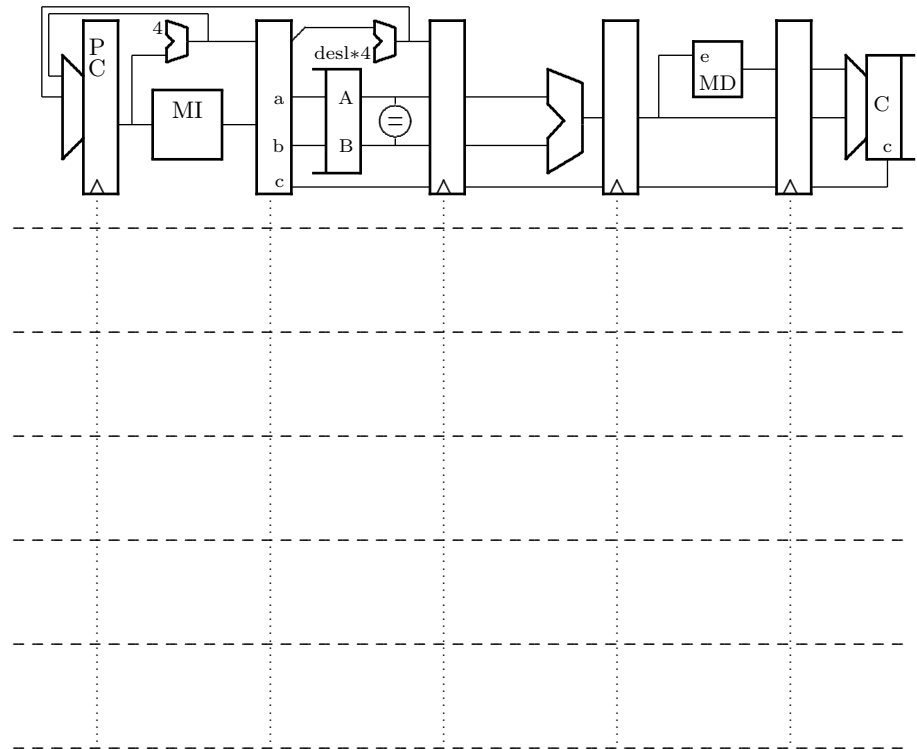
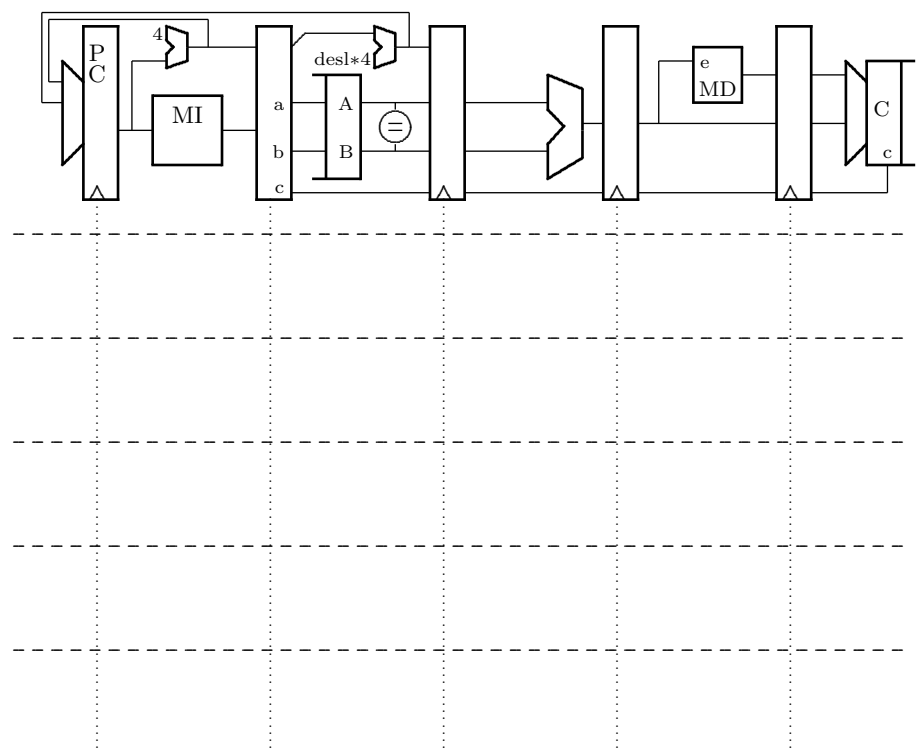




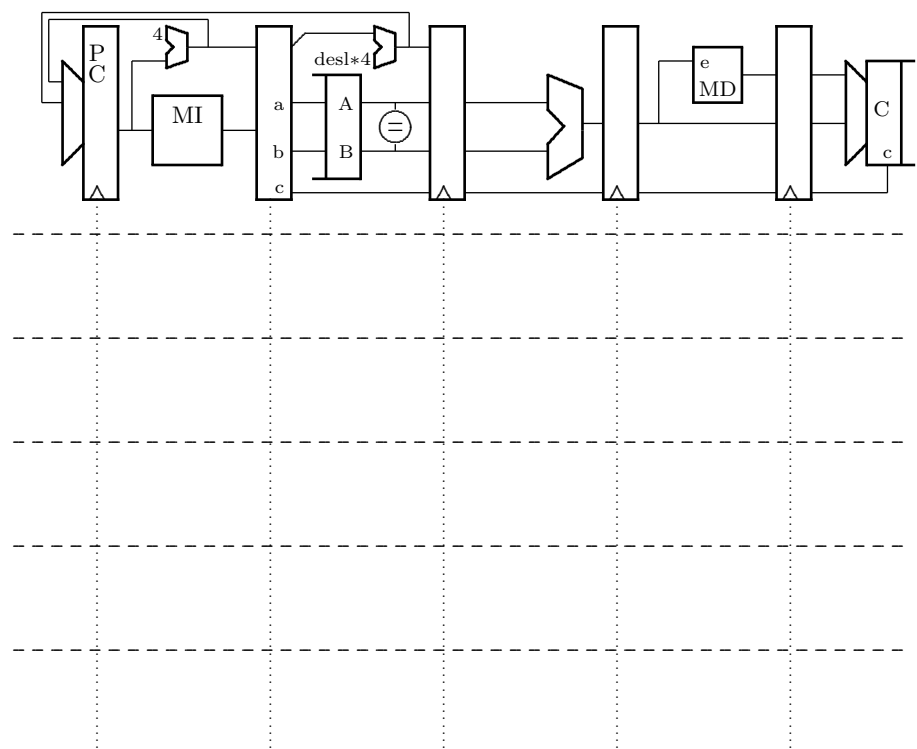
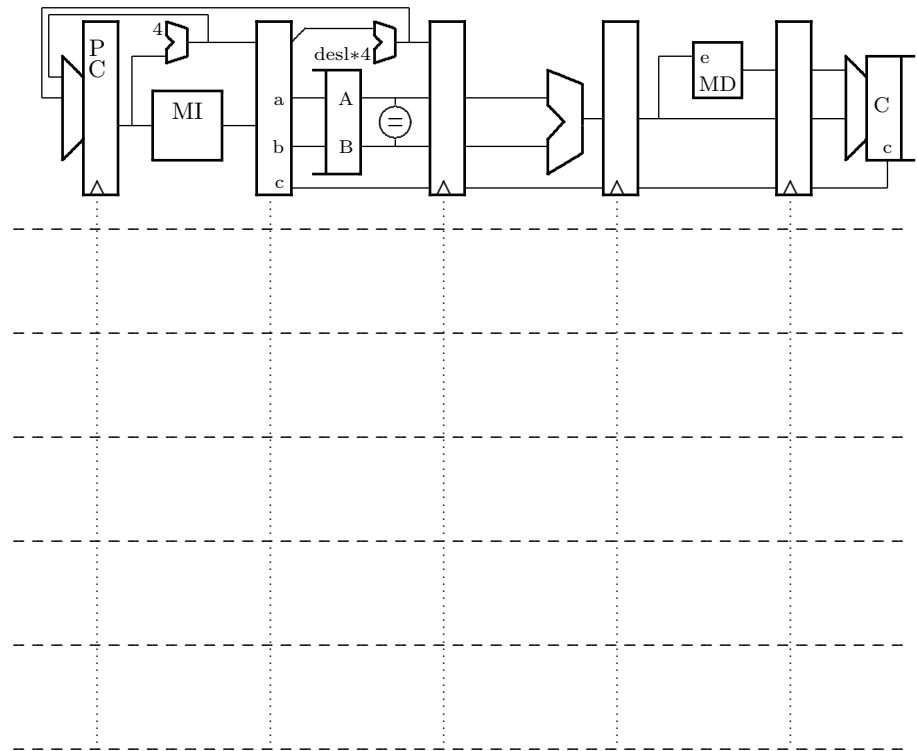
Ex. 1

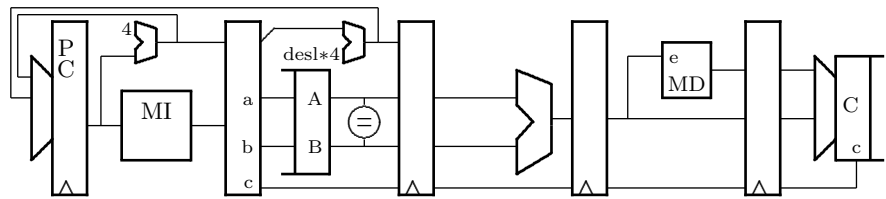
```
add r1, r2, r3
sub r4, r5, r6
xor r7, r8, r9
or  r10, r11, r12
and r13, r14, r15
```



Ex. 2

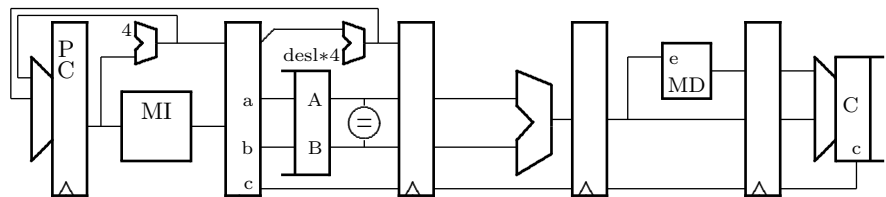
```
add r1, r2, r3
sub r4, r1, r6
xor r7, r4, r9
or  r10, r11, r7
and r13, r14, r10
```



**Ex. 5**

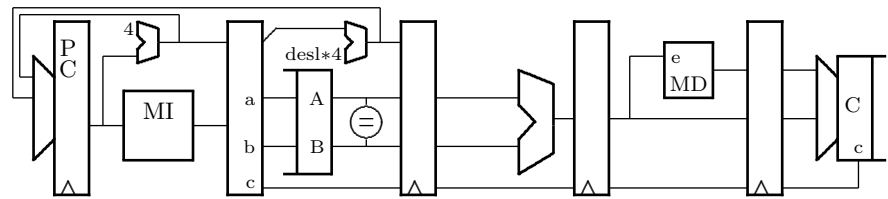
sem adiantamento

```
lw    r1, 0(r2)
addi  r2, r1, 1
sw    r1, 0(r4)
addi  r4, r4, 1
addi  r5, r5, -4
bne   r5, zero, -6
```

**Ex. 6**

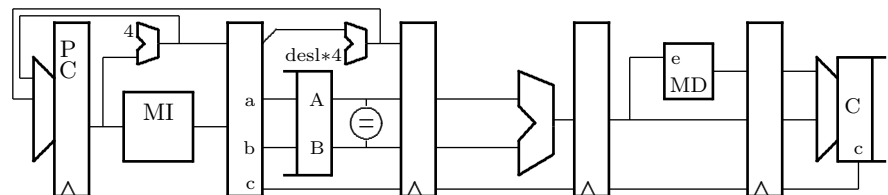
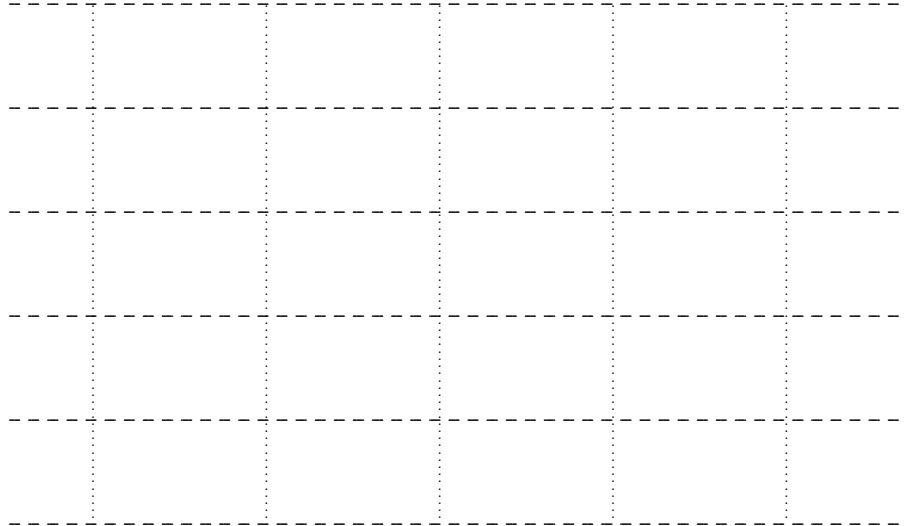
com adiantamento

```
lw    r1, 0(r2)
addi  r2, r1, 1
sw    r1, 0(r4)
addi  r4, r4, 1
addi  r5, r5, -4
bne   r5, zero, -6
```

**Ex. 7**

sem adiantamento
com reordenação

```
lw    r1, 0(r2)
addi  r2, r1, 1
sw    r1, 0(r4)
addi  r4, r4, 1
addi  r5, r5, -4
bne   r5, zero, -6
```

**Ex. 8**

com adiantamento
com reordenação

```
lw    r1, 0(r2)
addi  r2, r1, 1
sw    r1, 0(r4)
addi  r4, r4, 1
addi  r5, r5, -4
bne   r5, zero, -6
```

